Implementation of Encoding Circuit for Inverse Differential Manchester Code (IDMC) And Clock Recovery Circuit

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Abstract

In this research an inverse differential Manchester code (IDMC) circuit is implemented to encode random data using logical circuits, and clock recovery circuit is implemented too. A design of the first stage of clock recovery circuit which represents an edge detector circuit has been implemented using two one-shot mono-stable (74121) to detect the rising and falling edges respectively.

The two circuits are tested practically at a low bit rate (1Kb/s) to study there operations. The encoding and clock recovery processes observed using oscilloscope. A comparison is made using simulation program (MATLAB 7.4) with the practical results and they were close to simulation results. The encoded circuit has been tested at (5Mb/s) which is lying in Token ring LAN range.

In this research a practical illustration of the effectiveness of high pass filtering on random data has been made and compared with IDMC encoded data, this comparison improve the advantages of line code that have dc balance and high transition density which are lack in the random data.

Keywords: Line Code, Inverse Differential Manchester encoder circuit, clock recovery, practical implementation.

تنفيذ دائرة التشفير (IDMC) ودائرة استرجاع نبضة التوقيت (Clock)

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الملخص

في هذا البحث تم تنفيذ دائرة (IDMC) لتشفير البيانات العشوائية باستخدام الدوائر المنطقية، وأيضا تنفيذ دائرة استرجاع نبضة التوقيت (clock recovery). تم تصميم المر+حلة الأولى من دائرة استرجاع نبضة التوقيت وهي دائرة كاشف الحافات (edge detector circuit) باستخدام اثنين من أحادي الإستقرارية (One-Shot Mono-Stable) (74121) لكشف الحافات الصاعدة والنازلة على التوالي.

تم فحص عمل الدائرتين المنفذتين عمليا عند معدل قليل لنقل للبيانات (1Kb/s) لدراسة عمل الدائرتين. تم ملاحظة عملية التشفير وعملية استرجاع نبضة التوقيت باستخدام راسمة الذبذبات. أجريت مقارنة باستخدام برنامج المحاكاة(MATLAB 7.4) مع النتائج العملية وكانت مقاربة للنتائج العملية. تم فحص أداء دائرة التشفير عند (5Mb/s) حيث أنها تقع ضمن المدى الذي يُعمَل به في(Token ring LAN).

وتم في هذا البحث أيضا توضيح تأثير مرشح الترددات العالية على البيانات العشوائية عملياً ومقارنتها مع البيانات المشفرة (IDMC)، حيث أثبتت المقارنة فائدة تشفير البيانات لامتلاكها خاصية التوازن للمركبة المستمرة (dc balance) وكثافة انتقال عالية اللتان تكونان مفقودتان في البيانات العشوائية.

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1-INTRODUCTION:

Line codes are used in pulse code modulation (PCM) systems, satellite communication systems, magnetic recording systems, and in fiber optic data links.

The differential Manchester code was first introduced in 1998 is level insensitive, self-clocking coded since there is always at least one transition per bit cell, and hence the absence of un expected transition can be used for error detection to indicate logical value. Differential Manchester requires two signal changes to represent binary 0 but only one to represent binary 1 [1][2][3].

Because only the presence of a transition is important, polarity is not. Differential coding schemes will work exactly the same if the signal is inverted (wires swapped) [4].

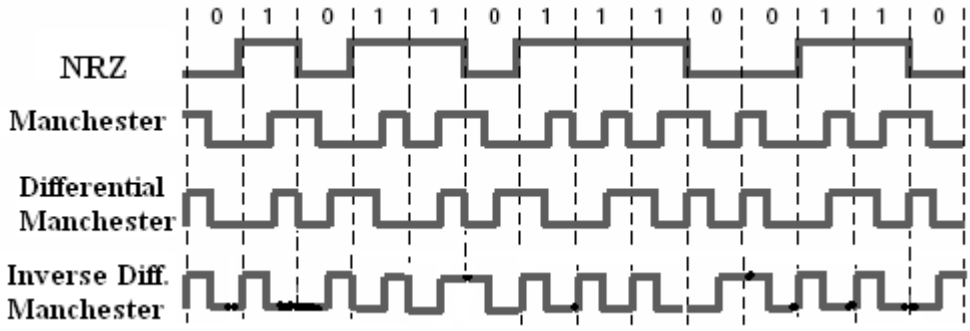


Fig. 1 Manchester codes timing diagram

From fig.1, for IDMC (the lower trace), in the middle of the bit-time there is always a transition, whether from high to low, or low to high [5].

The differential Manchester code is used in a number of communication and Electronic systems and it was adopted by IEEE to be used in the physical layer in Token Ring Local Area Networks [6].

2-Encoding circuit:

Fig.2 shows IDMC encoder circuit. The AND gate masks out the extra transition when the data is a '0'. The encoded data is obtained from the Q output of the JK-type flip-flop.

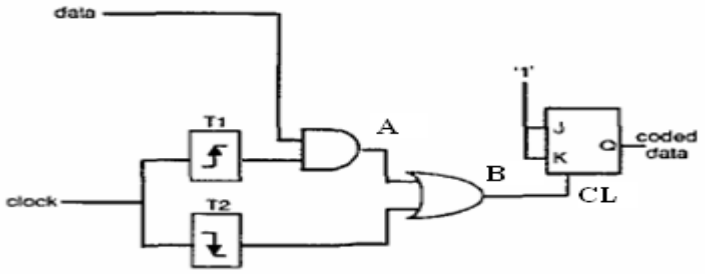


Fig. 2 IDMC encoder circuit

The two one shots T1 and T2 are used as clock transition detectors, T1 for positive transitions and T2 for negative ones. The output pulse duration of T1 and T2 one shots ($\tau_1 and \tau_2$) are selected such that [1]:

$\tau_1 = \tau_2 = \tau << T$ -----(1)

where $T=1/f_{clock}$.

A simple edge detection circuits shown in Fig.3 and Fig.4 respectively [6][7]. Here c' is delayed version of the clock signal c. Obviously,

T1=c. $\bar{c}'$, as shown in Fig.3

T2= c'. $\bar{c}$, as shown in Fig.4

Where "." denotes the logical AND operation and the over bar denotes the logical inverse operation.

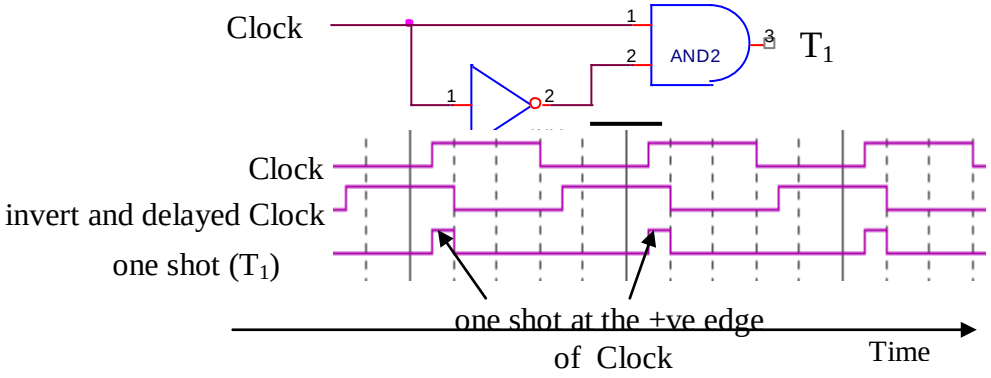


Fig.3. Rising edge detection circuits.

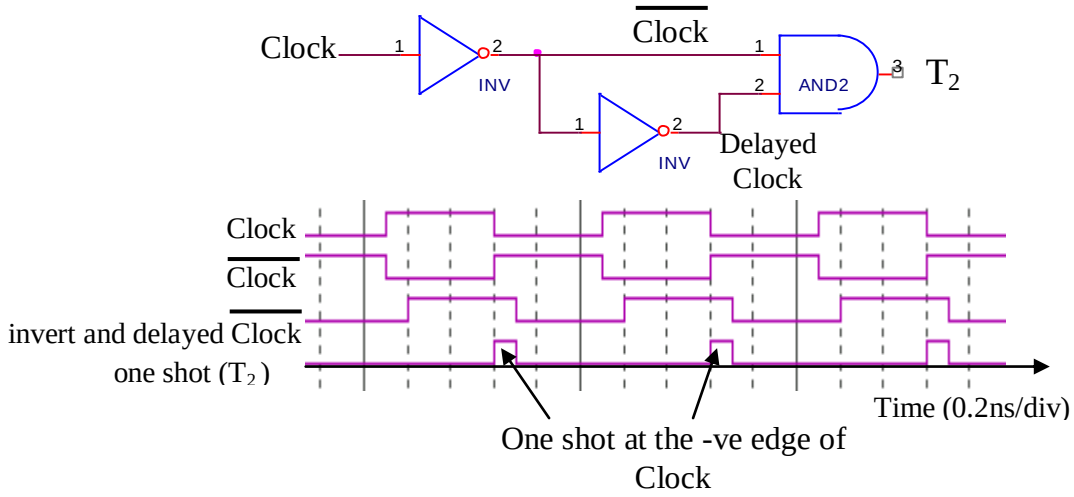


Fig. 4. Falling edge detection circuit and timing diagram.

The operation of the encoder is shown with the aid of timing diagrams in Fig.5 which presents the coded signal together with intermediate waveforms at each stage of the encoder for a test data pattern of 10111100.

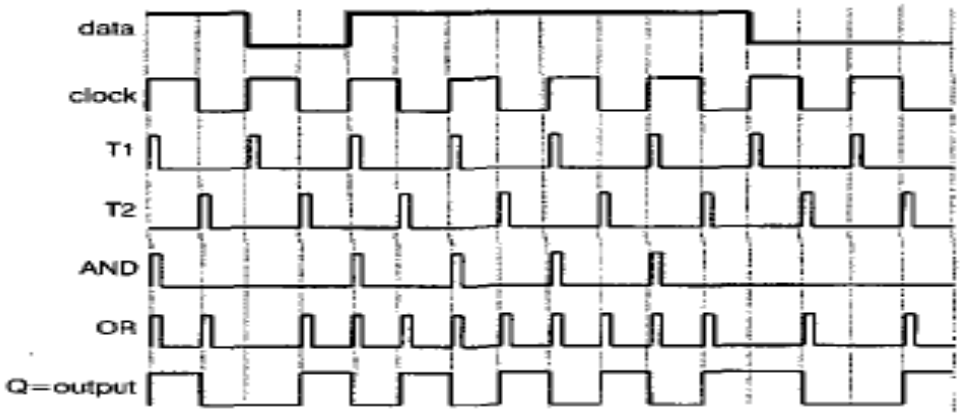


Fig. 5. IDMC timing diagram

3-Effect of High Pass Filtering (HPF) :

To understand the effect of high-pass filtering, suppose a random binary sequence is applied to a first –order RC section Fig.6, the output levels my "droop" significantly for long runs. As result, the bits after each long run suffer from a large (temporary) dc shift, making it difficult to set a decision threshold.

The above effect is called"dc wander" because the "instantaneous" dc value of the output waveform (V_1) continues to change randomly. To minimize dc wander, the time constant τ =RC must be sufficiently greater than the longest permissible run to ensure negligible droop, if the cutoff frequency of the HPF can not be change by the user a line code (like IDMC) must be used to minimize dc wander [8], (when a signal is received at the receiving terminal, the DC loss inside the transformer (so as HPF) would cause the phenomenon of signal level wander this called dc wander)[9] as shown in Fig.6 .

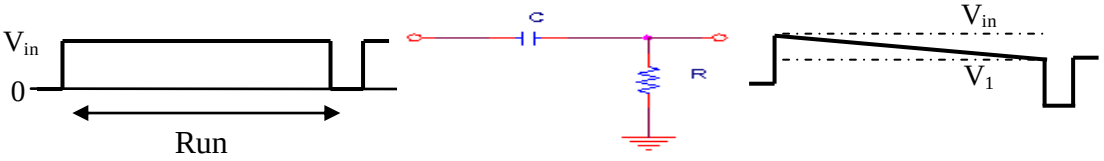


Fig.6 Example of droop in random data due to high pass filtering

4-Decoding circuit [10][11]:

The prior art methods of decoding phase encoded binary signal is presented in Fig.7. The clock decoder operates with a local clock that is closely matched to the transmitter clock embedded in the phase encoded signal, accepts the input signal and
operates on the state transition of the input signal to produce at its output a signal RXC, which is representative of the original transmitter clock embedded in the encoded data, RXD represent the original data.

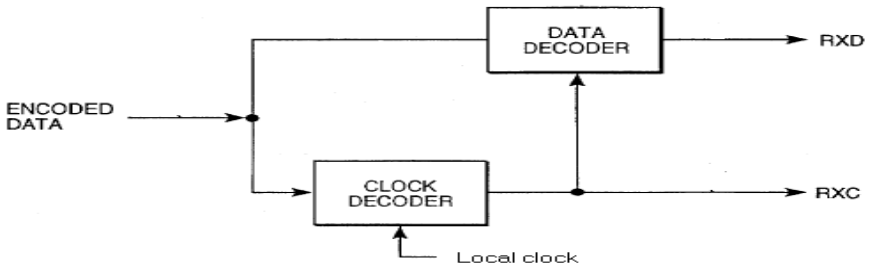


Fig.7 Decoding circuit

The recovered clock is used to determine the proper phase location at which to sample the data stream for recovery of the encoded data.Fig.8 shows a one-shot clock decoder that includes an edge detector operating on the binary input signal and generating a pulse for each signal state transition, AND-gate for gating out bit-cell boundary transitions and passing center bit-cell transitions to one shots (1/4 bit time) and (1/2 bit time), and inverter for clock waveform generation which is output at terminal as RXC and fed back to AND-gate through inverter.

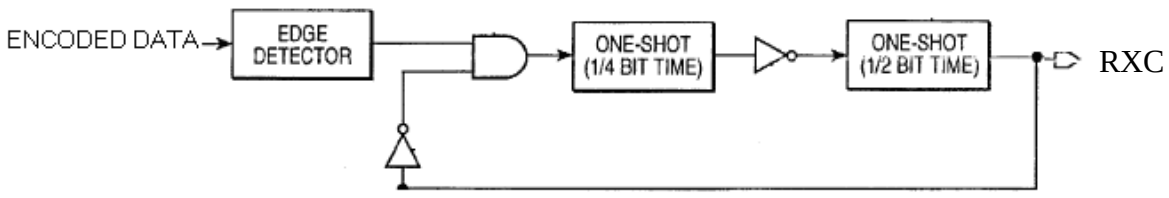


Fig.8 Clock recovery circuit using a one-shot as local clock

There are many different architectures for clock recovery. In measurement equipment, the most common type is based on a phase locked loop (PLL) Fig.9.[11]

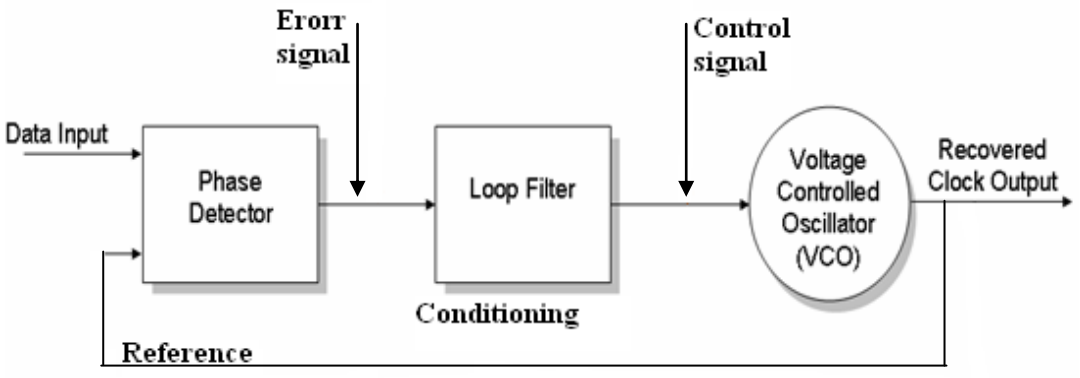


Fig.9 PLL Block Diagram

A Voltage Controlled Oscillator (VCO) free-runs initially, near the data rate of interest. A portion of the VCO signal forms one input to a phase detector. The other input to the phase detector is the incoming data. The phase detector compares the phases of the two inputs and produces
an output voltage related to the phase difference (the 'Error Signal' above).Usually this signal is filtered in some way before it becomes the frequency control voltage of the VCO.
Fig.10 shows a PLL type of clock decoder. The PLL clock decoder has the advantage of being able to track slow changes in the received clock rate.

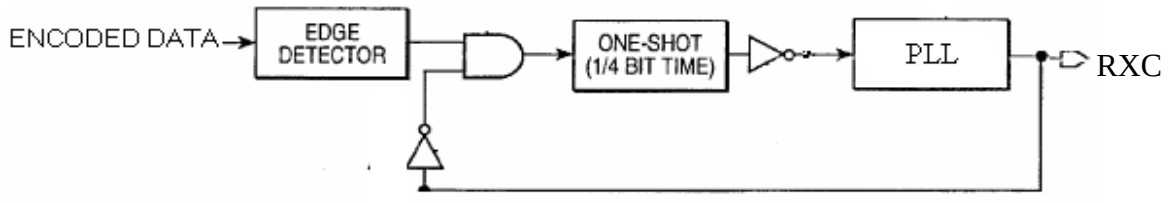


Fig.10 Improved Clock recovery circuit using PLL

5-Encoder implementation and testing:

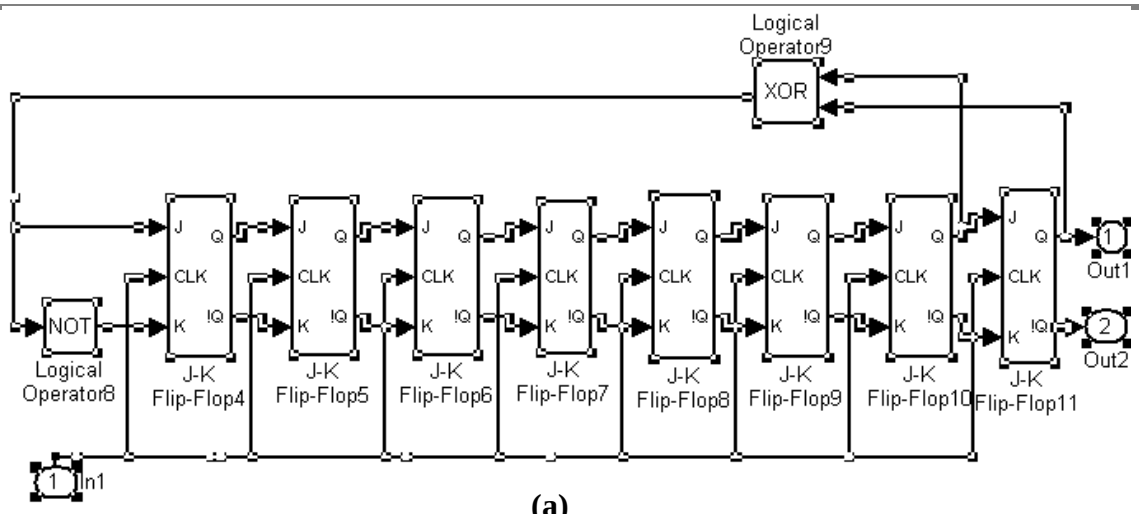
Fig.11.a represents the random data to be encoded using the IDMC circuit. The operation of the encoder in Fig.11(b) is shown with the aid of timing diagrams in Fig.12 which presents the coded signal together with intermediate waveforms at each stage of the encoder for a test data pattern of 101000011.

A=T1. Data

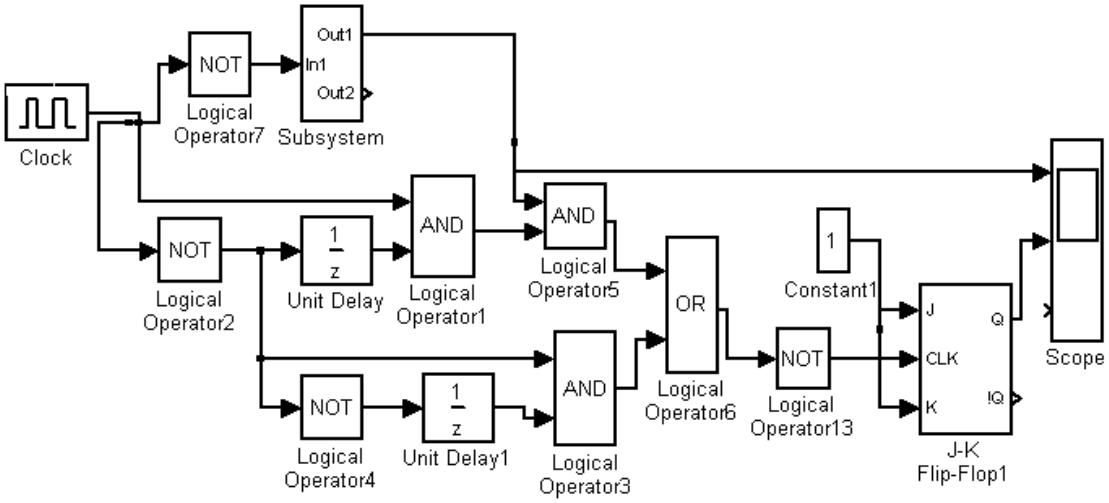
B=A $\cup$ T2

Where "$\cup$ " denotes logical OR operation[5]

The test pattern used here is selected such that it is representative of random bits of data and to check the effect of consecutive ones or zeros on the encoder operation.



(a)



(b)

Fig.11 (a) Random data to be encoded (b) IDMC circuit using Matlab

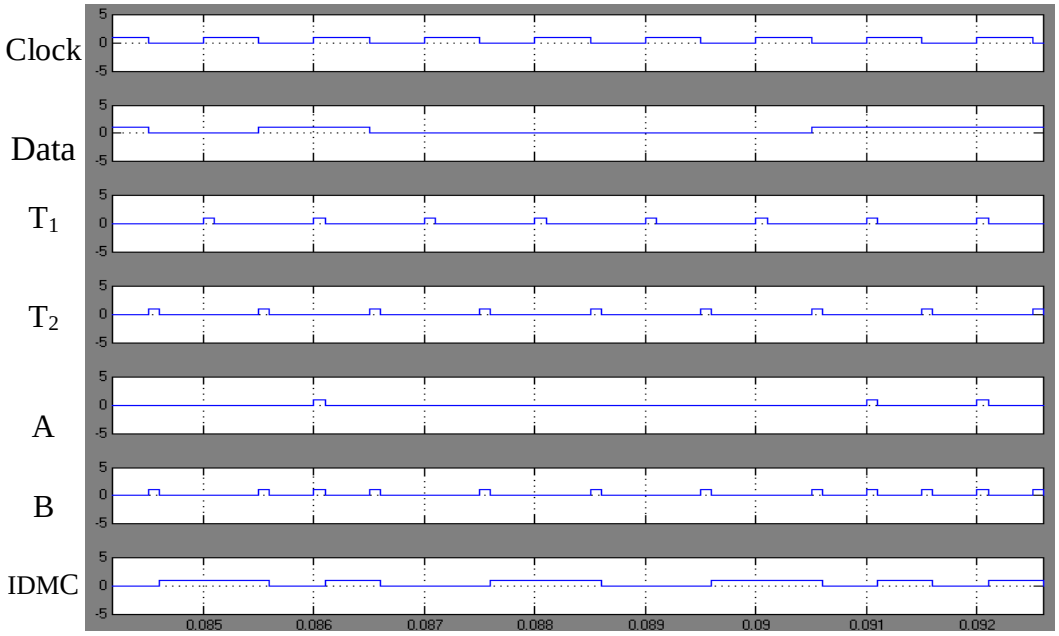


Fig.12 Timing diagram of IDMC using Matlab

The encoder was built in the laboratory, using standard transistor-transistor logic (TTL) integrated circuits. For testing purposes, a maximum operating frequency 5MHz was chosen, which sets equation(1): $\tau_1 = \tau_2 = \tau = 188ns$ as shown in Fig.13, while reference [1] reported the output pulse duration of the one shots to be $\tau_1 = \tau_2 = \tau = 5\mu s$.

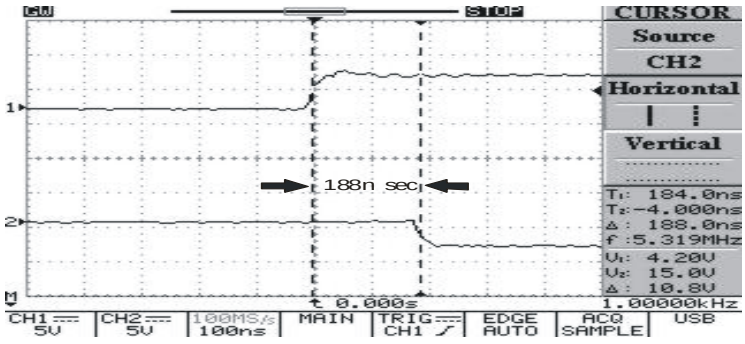


Fig. 13 The upper trace is the clock signal, the lower represent delayed clock

Practical results are shown in Fig.14, which contrasts the test pattern data and encoded output. The data pattern was tested and it was found that the encoder was able to encode the data correctly, the clock was varied between 1kHz and 5MHz without affecting the encoded data, which are close to simulation results using Matlab shown in Fig.12 ,while the clock for reference [1] was varied between 3 16 Hz and 95.21 kHz without affecting the encoded data.

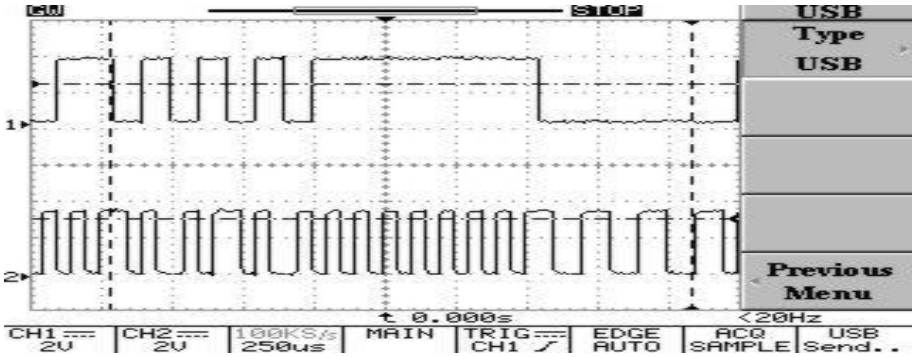


Fig. 14 The upper trace represent test pattern data signal the lower trace is the IDMC signal (practically)

A test has been made on the IDMC implemented circuit at 5M bps as shown in Fig.15.

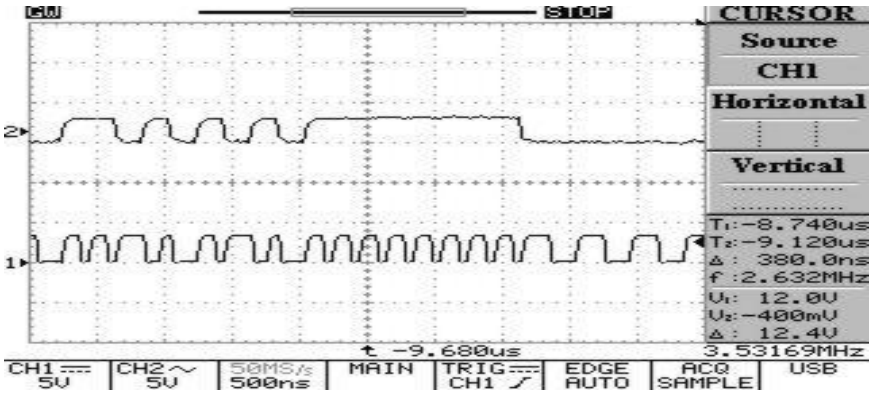


Fig15. The upper trace is data pattern and the lower is IDMC(practically)

6-Illustrate the effect of high pass filtering:

Fig.16(a) show a first order HPF using PSPICE(2006) simulation program, the effective of HPF on random data was shown in Fig.16(b), the lower trace show a (1V) voltage drop for (Vo) after the long run (8 bit) .The data pattern of Fig.14 (upper trace) is applied to a first order high pass filter of (R=8KΩ, C=1μF) to illustrate the advantages of encoding process, the time constant for the HPF is:

$\tau = R.C = 8$ msec

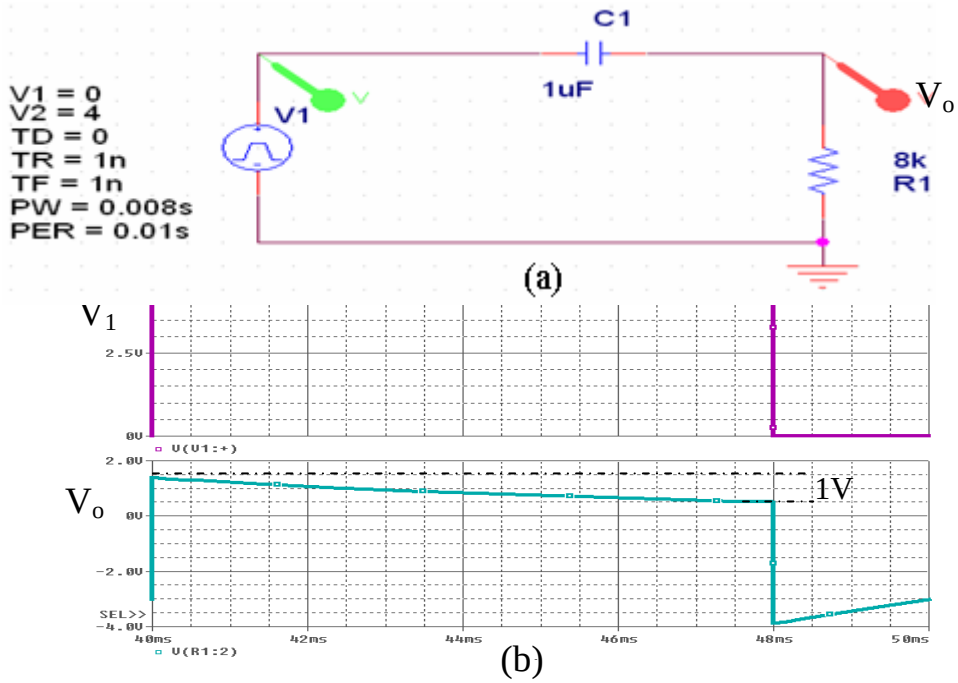
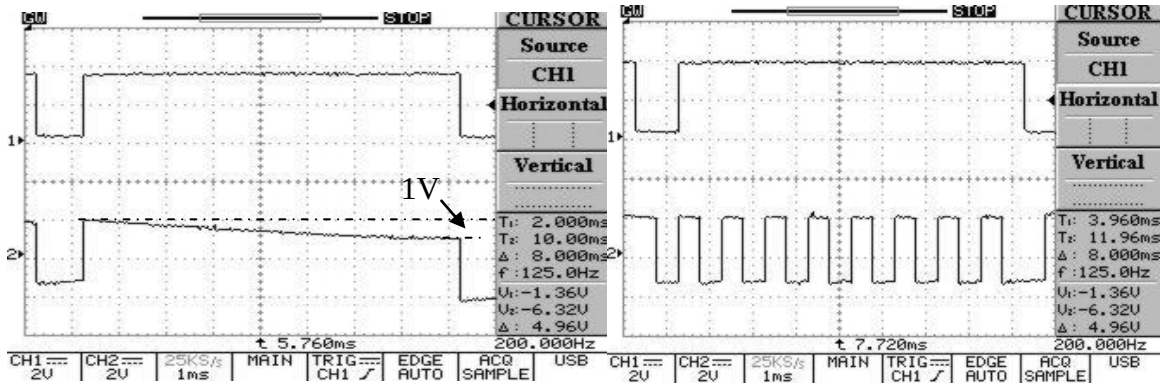


Fig.16 (a) first order HPF.(b) the waveforms of HPF

The practical results of the effective of HPF on random data (1V voltage drop at V_o due to long run) shown in Fig.17.a is close to simulation result in Fig.16.

We saw that the signal in Fig.17.b have dc balance (number of "1s"equal to the number of "0s") and high transition density that made easy to extract the clock signal from the data stream.



(a) (b)

Fig.17 The lower trace (a) dc wander at HPF output. (b) dc balance when use line code (IDMC).

7-Clock recovery implementation and testing:

The practical circuit of clock recovery utilities few digital components, OR, AND, NOT, and a mono-stable circuit .The theoretical timing diagram of this circuit is shown in Fig.18

Fig.19 represents the practical circuit description of clock recovery for IDMC using a mono-stable circuit (U4) as local clock regenerating (last stage). U1 and U2 represents rising and falling edge detector circuits respectively.

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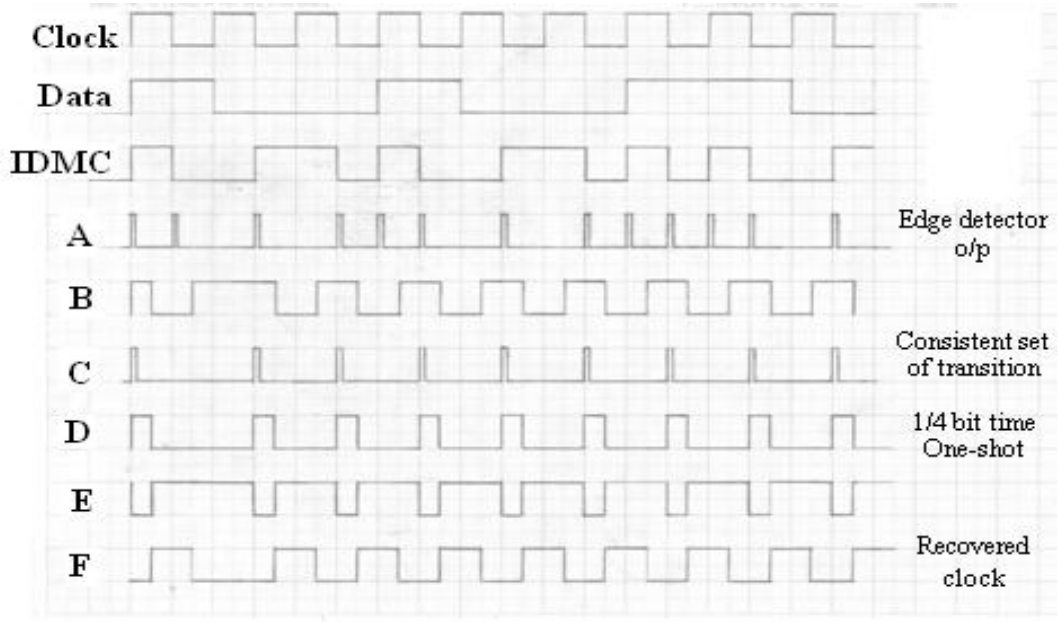

Fig. 18 Timing diagram of clock recovery circuit (theoretically)

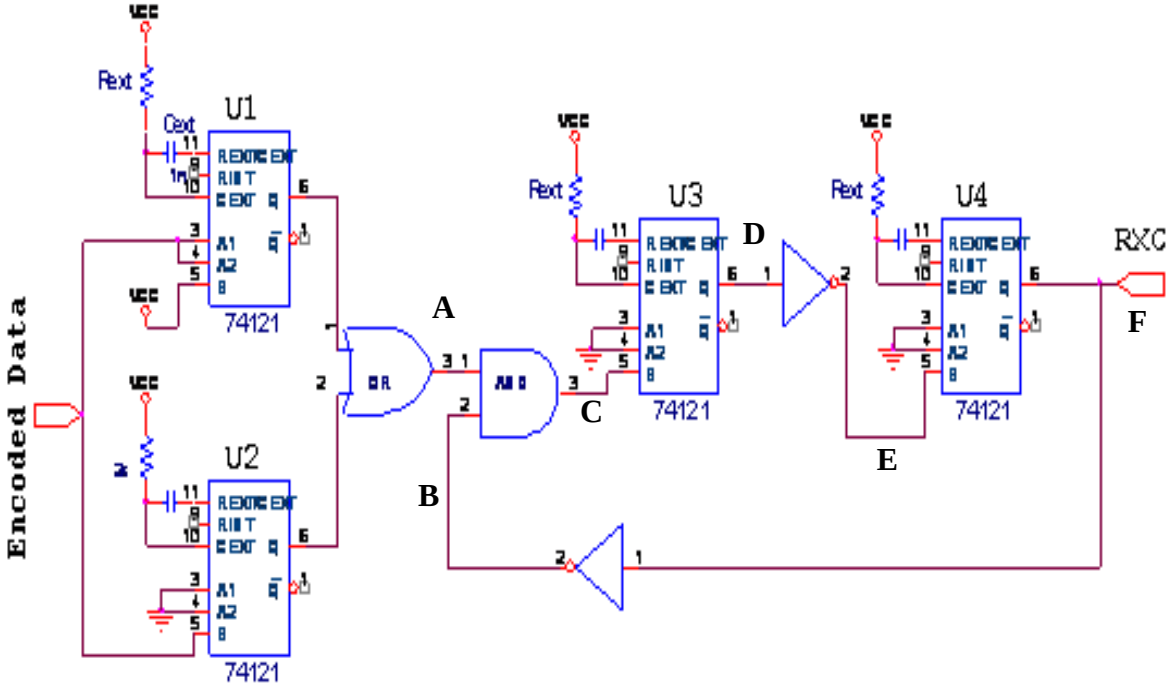

Fig.19 Clock recovery circuit using mono-stable 74121 (U4)

The timing diagram of the practical circuit is shown in Fig. 20.

The mono-stable (U4) in Fig.19 (last stage) is replaced by a phase locked loop (PLL) circuit (NE565) as a local clock regenerator. The PLL clock decoder has the advantage of being able to track slow changes in the received clock rate.

Fig.21 show the practical result of clock recovery circuit using PLL instead of mono-stable 74121. A test have been on the clock recovery circuit with PLL by changing the bit rat the PLL make a lock on the incoming signal frequency from 15.15KHz to 21.74KHz as shown in Fig.21 (a) and (b) respectively

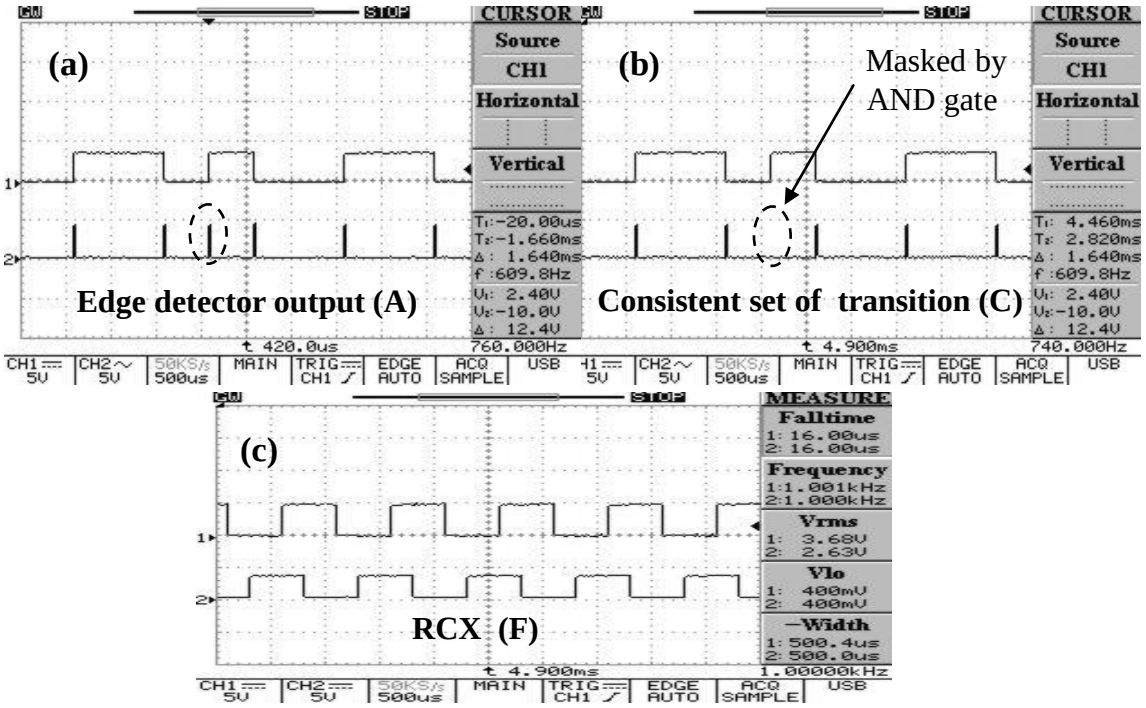

Fig.20 (practically). (a) The upper trace represent the encoded data, the lower trace is the output of edge detector (b) The lower trace is the output C (c) The upper trace represent the original clock the lower trace is the recovered clock.

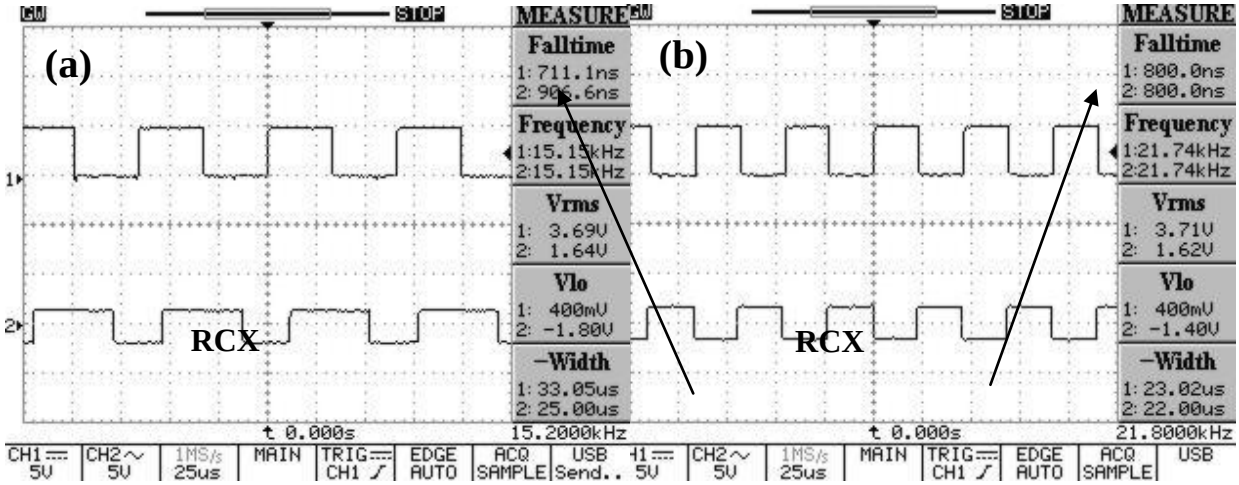

Fig.21 Original and recovered clock (a) at 15.15KHz, (b) at 21.74KHz (practically).

8-Conclusions:

An encoder circuit for Inverse Differential Manchester Code and a clock recovery circuit have been implemented. The hardware implementation utilizes one-shots for edge detector, OR gate, AND gate, and JK flip-flop. Once the encoder is set to operate at the highest possible frequency, the encoder can be operated at any other lower data rate.

The circuit was implemented in the laboratory using TTL technology, a test is made to the encoding circuit at 5Mb/s and it was found that the encoder was able to encode data correctly as same as matlab simulation results. A practical and simulation illustration of effectiveness of high pass filtering shows the advantages of encoding process. For accurate operation of edge detection circuit an external resistance and capacitance for (74121) are used as mentioned in its data sheet. The practical test of decoding process at (21.74KHz) using PLL show the concept of clock extraction from the encoded data.

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